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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/392,034	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-27,31-40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-27,31-40,42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after the Notice of Appeal. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 30, 2003 has been entered.

Status of the Claims

2. Amendment filed September 30, 2003 has been entered. Claim 2 has been canceled. Claims 1, 7, 13, 14, 18, 24-26, 31, 35, 38, 42 and 43 have been amended. Claims 1, 3-27, 31-40, 42 and 43 are pending.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "forming **said liner** upon side sidewall of said isolation trench comprises **deposition** of a composition of matter" (claim 4) No new matter should be entered.

With respect Fig. 8B, in Fig. **8B**, numeral "**44**" is used for the pad oxide layer, the correct number should be "**14**".

As discloses in the specification, the **gate oxide layer 44**, however, is only formed **after** the removal of the polysilicon island layer 24. (See page 19, lines 10-16, Fig. 9B).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 25, 34 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 25, lines 34-35, recites: "layer composed of polysilicon upon said **gate** oxide in contact with a pair of said spacers".

As shown in Fig. 7B, the polysilicon 24 is formed upon the pad oxide 14; further, the **gate** oxide 44 was **not** formed until all of the layers have been removed. (See page 19, lines 15-16).

Therefore, the correct term should be "layer composed of polysilicon upon said oxide layer".

Note that, there is only one layer of polysilicon 24 formed on the substrate 12 and being confined in the spacer between the isolation trenches 48, and that layer 24 is formed on **the pad oxide 14**. (See Figs. 2B-7B).

Response to Amendment

5. The amendment filed **February 14, 2002** is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "said planarizing is performed **in the absence** of masking the conformal layer over each said isolation trench".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1, 3-27, 31-40, 42 and 43 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which **was not described in the specification** in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a **written description** of the claim limitation "planarizing is performed **in the absence** of masking the conformal layer over each said isolation trench" in the application as filed. The same had been rejected in the previous Office Action.

MPEP 2173.05(i) states: "The mere absence of a positive recitation is **not** basis for an exclusion. Any claim containing *a negative limitation* which *does not have basis in the original disclosure* should be rejected under 35 U.U.C. 112, first paragraph as failing to comply with the

written description requirement". (See *In re Schechter,* 205 F.2d 185, 98 USPQ 144 (CCPA 1953); *Ex parte Parks*, 30 USPQ2d, 1234, 1236 (Bd. Pat. App. & Inter. 1993).

Applicant should point out a specific portion of the original specification that directs to "planarizing is performed **in the absence** of masking the conformal layer".

7. Claims 4, 16 and 21 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "**rounding the top edge of the trench**" by thermally grown oxide from the substrate, does not reasonably provide enablement for *rounding the top edge of trench* by **depositing material** on the trench surface. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

The specification clearly indicated that the rounding of the edge at the top of the isolation trench is a result of thermal oxidizing of the sidewall 50 to form the insulation liner 30. (See page 12, 1st paragraph). Further, as an alternative, the insulation liner can be formed by CVD.

Note that, rounding of the corner is a result of thermal oxidation, forming the thermal liner. When the insulation liner forms by CVD, the CVD is deposited on the etched trench which have not been rounded by the oxidation. Therefore, depositing the insulation liner by **CVD** does not result in rounding the corner and rounding the corner is not formed by CVD.

The specification ***fails to provide support*** for rounding the top edge of the trench by depositing material (CVD).

It is well known in the semiconductor technology that by consuming silicon at the corner during the thermal oxidation, the top edge of the trench becomes rounded.

Deposition, e.g. CVD, **does not consume any material** from the silicon substrate. Therefore, rounding does not occur.

How can the edge of trench be rounded when the liner is formed by deposit ?

8. Claims 16 and 23 are further rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for forming a thermal liner oxide 30 to be confined within each isolation trench, but does not reasonably provide enablement for the liner 30 being formed by deposit, e.g., CVD, to be confined within each isolation trench. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

How can a dielectric material which is formed by deposit be confined within the trench ?

Regarding the nature of CVD on the substrate, see Omid-Zohoor '108, Fig. 3I, oxide liner (58b), which is formed by deposit. (See col. 4, ll. 51-60)..

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1, 3-26 and 31-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation " wherein **material** that is electrically insulative extends continuously between and within said plurality of isolation trenches" in lines 28-29. There is insufficient antecedent basis for this limitation in the claim.

What is the "material" that the claim is directed to ?

Similar limitation is also recited in claims 7, 14, 18, 24, 25, 26 and 31.

Claim 35 recites the limitation " wherein **electrically insulative material** extends continuously between and within said plurality of isolation trenches" in lines 9-10. There is insufficient antecedent basis for this limitation in the claim.

What is the "electrically insulative material" that the claim is directed to ?

Similar limitation is also recited in claim 38.

10. Claims 9, 10, 12, 13, 26 and 27 are further rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 9, 10, 12, 13, 26 and 27 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the specification filed September 8, 1999. In the specification, page 14, lines 14-25, applicant has stated "*Figure 7A illustrates a subsequent step of formation of the isolation trench wherein insulator island 22, spacer 28, and isolation film 36 are planarized to a common co-planar first upper surface 38. First upper surface 38 will preferably be formed by a CMP or etchback process. Preferably, planarization will be selective*

to isolation film 36, and relatively slightly selective to insulator island 22, such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, selective to isolation film 36 as compared to insulator island 22. A more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred selectivity is about 1.5:1. Planarization also requires the etch recipe to be slightly selective to spacer 28 over insulator island 22.", and this statement indicates that the invention is different from what is defined in the claim(s) because said passage means: isolation film 36 is etch faster than the insulator island 22, while claim 9 recites: "wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said *first dielectric layer* (insulator island 22) *faster than said conformal layer* (isolation film 36) *and said spacers* (28) by a ratio in range from of about 1:1 to about 2:1.

Clearly, claim 9 is contradicting the disclosure, thus, fails to correspond to the scope of the invention.

Similar subject matter also recite in claims 10, 12, 13, 26 and 27.

As best understood by the examiner, the upper surface of each isolation trench is formed by an etch process using an etch recipe that etches the conformal layer 36 and spacers 29 faster than the insulator layer 22.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims **1**, 3-27 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor et al. (U.S. Patent No. 6,097,072) in view of Poon et al. (U.S. Patent No. 5,387,540) (all of record).

With respect to claim **1** and **14**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer (340); (Fig. 3C);

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas; (Fig. 3E);

forming a second dielectric layer (352) conformally over the oxide layer (340) and the first dielectric layer (344), wherein the forming the second dielectric layer (352) includes forming a second dielectric layer (352) over and in contact with the exposed oxide layer (340) at the plurality of areas; (Fig. 3G);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer (352), wherein each spacer is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas; (Fig. 3H);

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench (360) is adjacent to and below the pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench (360) has a top edge; (Fig. 3I);

filling each isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344); (Fig. 3J); and

planarizing the conformal layer (364) and each spacer (356) to form therefrom an upper surface for each isolation trench (376) that is co-planar to the other upper surfaces, wherein the planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of forming a liner upon the sidewall and rounding the top edge of the isolation trench (360).

However, Poon teaches that it is well known in the art to form a thermal liner (28) on the etched trench surface to remove damage caused by the trench-etch. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch. Further, the growing of the thermal liner is **inherently** resulted in rounding the top corner of the trench.

With respect to claim 3, the liner (28) of Poon is thermally grown oxide of the semiconductor substrate. (See Fig. 4).

With respect to claim 4, as best understood by the examiner, the liner (28) of Poon comprises deposition of a composition of matter (50). (See Fig. 11).

With respect to claim 5, Omid-Zohoor is shown to teach all the features of the claim with the exception of further includes forming a doped region below the termination of each isolation trench.

However, Poon further teaches forming a doped region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12). (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further form a doped region below the termination of each isolation trench within the semiconductor substrate of Omid-Zohoor as taught by Poon to prevent the inversion.

With respect to claim 6, the upper surface for each isolation trench (376) of Omid-Zohoor is formed by CMP. (See Fig. 3M, col. 4, ll. 47-62).

With respect to claim 7, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer (340) and the first dielectric layer (344);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench is adjacent to and below the pair of the spacers (356) and is situated at the corresponding area of the plurality of areas;

filling each the isolation trench with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with the corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal layer and the depositing is carried out to the extent of filling each of the isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing with a single etch recipe the conformal layer (364) to form therefrom an upper surface for each of the isolation trench that is co-planar to the other upper surfaces, wherein:

the planarizing is performed in the absence of masking the conformal layer (364) over each of the isolation trench;

material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

the conformal layer (364) and the spacers (356) form the upper surface for each isolation trench, each upper surface being formed from the conformal layer and the spacer and being situated above the pad oxide layer (340); and

the first dielectric layer (344) is in contact with at least a pair of the spacers (356) and the pad oxide layer (340). (See Figs. 3A-M).

With respect to rounding the top edge of each isolation trench, the similar reason as that of claim 1 is also applied here.

With respect to claim 8, the method of Omid-Zohoor '072 further includes:

removing the pad oxide layer (340) upon a portion of the surface of semiconductor substrate (120); (Fig. 3O); and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate. (See Fig. 3P).

With respect to claims 9 and 10, as best understood by the examiner, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed in an etch process using an etch recipe that etches the conformal layer (372) faster than the first dielectric layer (344).

With respect to claim 11, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed including:

chemical mechanical planarization, CMP, wherein the conformal layer (364), the spacers (356), and the first dielectric layer (344) form a planar first upper surface; (Fig. 3M); and

an etch that forms a second upper surface, the second upper surface being situated above the pad oxide layer (340). (Fig. 3N).

with respect to claims 12 and 13, as best understood by the examiner, the etch that forms a second upper surface is well known in the art to etch the first dielectric layer (344) faster than the conformal layer (364) and the spacers (356).

With respect to claim **14**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) upon the oxide layer (340);

selectively removing the silicon nitride layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a first silicon dioxide layer (352) over the oxide layer and the silicon nitride layer, wherein the forming of the first silicon dioxide layer (352) includes forming a first silicon dioxide layer (252) on and in contact with the exposed oxide layer (340) at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer is situated upon the oxide layer

(340), is in contact with the silicon nitride layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into and terminating within the semiconductor substrate (120), wherein each isolation trench (360) is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

filling each isolation trench (360) with a conformal second silicon dioxide layer (364), the conformal second silicon dioxide layer within each isolation trench extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second silicon dioxide layer (364), and the depositing is carried out to the extent of filling each isolation trench and extending over the spacers (356) and the silicon nitride layer (344); and

selectively removing the conformal second silicon dioxide layer (364) and the spacers (356) to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above the oxide layer (340), wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches, and wherein the selectively removing is performed in the absence of masking the conformal second dioxide layer (364) over each isolation trench. (See Figs. 3A-M).

With respect to forming an electrically active region below the termination of each isolation trench (or doped region) and rounding the top edge of each isolation trenches, respectively, the similar reasons as that of claims 5 and 1, respectively, are also applied here.

Note that, the formation of the thermal liner (28) is inherently result in rounding of the top edge of the isolation trench.

With respect to claim 15, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim 16, as best understood by the examiner, the liner of Poon is also composed of silicon nitride (50).

With respect to claim 17, the process of Omid-Zohoor '072 further includes:

removing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (Fig. 3O); and

forming a gate oxide layer (380) upon the portion of the surface of semiconductor substrate (120). (See Fig. 3P).

With respect to claims **18** and **24**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352)

includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein planarizing the conformal third layer (364) to form therefrom the upper surface for each isolation trench that is co-planar to the other upper surface further comprises planarizing the conformal third layer (364) and each spacers (356) to form therefrom the co-planar upper

surfaces, and the planarizing the conformal third layer is performed in the absence of masking the conformal third layer (364) over each of the isolation trench; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trench. (See Figs. 3A-M).

With respect to rounding the top edge, the similar reason as that of claim 1 is also applied here.

Further, although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended to form the spacers (356) on the thermally-grown oxide layer (34). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to claim 19, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed by CMP.

With respect to claim 20, a similar reason as that of claim 5 is also applied here.

With respect to claim 21, the process of Omid-Zohoor '072, in view of Poon, further comprises: prior to filling each isolation trench with the conformal third layer (364), forming a liner (28) upon the sidewall of the isolation trench to remove damage caused by the trench etch, the liner (28) being confined preferentially within each isolation trench (Fig. 4) and extending from an interface thereof with the oxide layer (340) to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third layer (364) is composed of electrically insulative material.

With respect to claim 22, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim 23, as best understood by the examiner, forming the liner upon the sidewall of the isolation trench of Poon also comprises deposition of a composition of matter (50).

With respect to claim **25**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface, wherein the planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench;

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120);

forming in between the isolation trench, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Fig. 3A-M).

With respect to rounding the top edge, the similar reason as that of claim 1 is also applied here.

With respect to removing the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim **26**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) by an etch using an etch recipe that etches the first dielectric layer (344) slower than the conformal third layer (364) and the spacers (356) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper

surface, wherein the planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364) and the plurality of isolation trench. (See Figs. 3A-M).

With respect to rounding the top edge, the similar reason as that of claim 1 is also applied here.

With respect to removing the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim 27, as best understood by the examiner, in the planarizing of the conformal third layer (364), the conformal third layer is remove faster than the first dielectric layer (344). (See Fig. 3M).

With respect to claim **31**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming a pad oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a silicon nitride layer (344) upon the polysilicon layer;

selectively removing the silicon nitride layer (344) to exposed the pad oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) conformally over the pad oxide layer and over the silicon nitride layer (344), wherein the forming of the first silicon dioxide layer (352) includes forming the first silicon dioxide layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer (356) is situated upon the pad oxide layer, is in contact with the silicon nitride layer (344) and the polysilicon layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal second layer (364), the conformal second layer extending above the pad oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the silicon nitride layer (344); and

planarizing the conformal second layer (364) and each of the spacers (356) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface and is situated above the pad oxide layer (340), wherein the planarizing is performed in the absence of masking the conformal second layer (364) over each of the isolation trenches;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

With respect to removing the silicon nitride layer and the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to forming of the doped region, the liner and rounding the top edge of the isolation trench, the similar reasons as that of claims 1 and 5 are also applied here.

With respect to claim 32, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 33, as best understood by the examiner, the liner of Poon is also composed of silicon nitride (50) and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 34, as best understood by the examiner, the method of Omid-Zohoor further comprises: (also see claim 25):

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (see Fig. 3N);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120); (see Fig. 3P);

forming in between the isolation trench, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces. (See Fig. 3N).

12. Claims **35**-40, **42** and **43** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Wolf *Silicon Processing for the VLSI Era*, Vol. 2, pp. 54-55 (of record).

With respect to claim **35**, as best understood by the examiner, Omid-Zohoor teaches a method of forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer; (col. 4, ll.14-16);

forming a first layer (344) upon the polysilicon layer;

selectively removing the first layer (344) and the polysilicon layer to expose the oxide layer at a plurality areas;

forming a plurality of isolation trenches (360) through the exposed oxide layer at the plurality of areas, wherein electrically insulative material (364) extends continuously between and within the plurality of isolation trenches, each isolation trench (360):

having a spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer in contact with the spacer (356), wherein the filling is performed by depositing the second layer, and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first layer (344);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer, wherein the planar upper surface is formed by planarizing in the absence of masking the second layer over each of the isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of the top edge of the isolation trench being rounded.

However, Wolf teaches that it is well known in the art to form a rounded top edge of the isolation trench by forming a thermal liner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Wolf to remove damage caused by the trench etch. Further, the rounding the top corner of the trench is an inherent result of thermally oxidizing the surface of the trench.

With respect to selectively removing the first layer and the polysilicon layer to exposed the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim 36, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 2-37).

With respect to claim 37, the doped trench bottom of wolf has a width which is greater than the width of the respective isolation trench. (See Fig. 2-37).

With respect to claim **38**, as best understood by the examiner, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon; (Fig. 3B);

forming a first layer (344) upon the oxide layer; (Fig. 3C);

selectively removing the first layer (344) to expose the oxide layer (340) at a plurality of areas; (Fig. 3E);

forming a plurality of isolation trenches (360) through the oxide layer at the plurality of areas, wherein electrically insulative material (364) extends continuously between and within the plurality of isolation trench, each isolation trench (360):

having a spacer (356) composed of dielectric material upon the oxide layer (340) in contact with the first layer (344); (Fig. 3H);

extending from an opening thereto at top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the spacer (356); (Fig. 3I);

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer (340) in contact with the spacer (356), wherein the filling is performed by depositing the second layer (364), and the depositing is carried out to the extend of filling each isolation trench and extending over the spacer (356) and over the first layer (344); (Fig. 3J);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer (340); wherein the planar upper surface is formed by planarizing in the absence of masking the second layer (364) over each of the isolation trench; (Fig. 3M); and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches. (See Figs. 3A-M).

With respect to the top edge being rounded, a similar reason as that of claim 35 is also applied here.

With respect to claim 39, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of isolation trenches. (See Fig. 2-37).

With respect to claim 40, the doped trench bottom of wolf has a width which is greater than the width of the respective isolation trench. (See Fig. 2-37).

With respect to claim **42**, As best understood by examiner, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a polysilicon layer upon the oxide layer; (col. 4, ll. 14-16);

forming a first layer (344) upon the polysilicon layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

a first isolation trench (360) extending from an opening thereto at the top edges at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures (360), wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of filling each isolation trench and extending over the spaces (356) and the first layer (344); and

forming with a single etch recipe a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

With respect to rounding the top edge of the isolation trench, a similar reason as that of claim 35 is also applied here.

With respect to claim **43**, as best understood by examiner, Omid-Zohoor teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344);

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures, wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of filling each isolation trench and extending over the spaces (356) and the first layer (344); and

planarizing the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures to form a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of respective first and second isolation structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

With respect to the rounding of the top edges of the isolation trench, a similar reason as that of claim 35 is also applied here.

Response to Arguments

13. Applicant's arguments filed September 30, 2003 have been fully considered but they are not persuasive.

Objection to the Drawings

Fig. 5A and 5B, only show a liner (30) which are formed by thermally grown, not deposit. As discussed above, a liner if formed by deposit, should extend over the substrate as shown in Fig. 3I of patent No. 6,184,108. The objection is maintained.

Objection under 37 CFR 1.75(c)

Referring to Fig. 8B, the Applicants state: wherein a polysilicon 24 is formed over a gate oxide 44.

However, Fig. 8B, as discussed above, the numeral 44 should be 14, because, up to that instant, the polysilicon 24, part of the mask (22/24/14) have not been removed. Fig. 8B, appears to be an enlargement subsequent to the removal of the etch stop layer 22. Therefore, the polysilicon layer 24 is only formed over the pad oxide 14, rather than the gate oxide 44, which is formed after the removal of the pad oxide 14 as shown in Fig. 9B. (See page 19, lines 10-16).

Objections under 37 U.S.C. 132

With respect to negative limitation e.g., "in the absence of masking", as discussed above, a positive recitation in the specification is required for a negative limitation claim.

The new matter objection is maintained.

Claim Rejection Under 35 U.S.C. 112, first paragraph:

Since the limitation "leaving no gap in" has been removed, the argument regarding that issue is moot.

Through a lengthy argument, applicant still fails to point out the specific disclosure regarding the planarizing is performed in the **absence** of masking the conformal layer, even the cited portion also fails as well.

As discussed above, a positive recitation in the specification is required for a negative limitation claim. (See MPEP 2173.05(i)).

With respect to claim 4, 16 and 21, applicant argues that the claims recite the formation of a liner and the step of rounding the top edge of the trench as a separate limitations.

Although the formation of a liner and the step of rounding the top edge of the trench seem to be a separate limitations. However, the specification discloses: "it can be seen that, following thermal oxidation, of sidewall 50 to form insulation liner 30 within isolation trench 32, semiconductor substrate 12 forms a rounded edge at the top of isolation trench 32. (Page 12, lines 4-6).

The specification breath life into the claim, therefore, what seem to be two separate limitations is actually one, which is the formation of the thermal liner 30. The CVD liner 30, as indicated as "another method", which means if formed by thermal grown, the liner 30 would result in a rounded top edge or as an alternative, if formed by CVD, the isolation trench would not have a rounded top edge.

Applicants assert that: enablement of "rounding the top edge of trench by depositing material on the trench surface" is not necessary.

However, claim 4 recites: "**wherein forming said liner** upon said sidewall of isolation trench comprises deposition of a composition of matter". As discussed above, claim 4 is interpreted as, forming said liner using deposit upon the sidewall of each isolation trench comprises deposition of composition of matter results in rounding the top edge of each of said isolation trenches".

Therefore, the enablement of CVD liner to form rounded top edge must be given and thus, maintained.

With respect to claim 16, the limitation of claim 14, in which claim 16 depends on, lines 19-20, recites: "said liner being confined preferentially within each said isolation trench". Claim 16 recites: "wherein said liner is composed of silicon nitride".

It is well known in the art that thermally grown oxide liner is confined within the isolation trench. (See instant Figs. 5A and 5B; Pat. No. 6,184,108, Fig. 3H and Pat. No. 5,387,540, Fig. 4).

"silicon nitride" of claim 16 is referring to CVD liner, an alternative method. It is also well known in the art that, a material forms by deposit would not be confined within the isolation trench. (See Pat No. '108, Fig. 3I, liner 58b; and '540, Fig. 11, liner 50).

Applicants clearly fail to prove that liner forms by CVD is confined within the isolation trench. The rejection of claim 16, as well as claim 23, is maintained.

Rejection Under 35 U.S.C. 112, second paragraph:

With respect to claims 1, 3-26 and 31-40, Applicant states: "As further depicted in Figure 5-8, it can be seen that this continuous material(s) is derived from the electrically insulative materials oxide layer 14".

In response to applicant's argument that the specification show certain features of claims, it is noted that the features upon which applicant relies (i.e., wherein material that is electronically insulative extends continuously between and within said plurality of isolation trenches) **are lacking antecedent**. **Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims**. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Reviewing the claimed terminology, one having ordinary skill in the art could not possibly know what the "**material** that is electronically insulative" is directed to.

The rejection is maintained.

With respect to claims 9, 10, 12, 13, 26 and 27, the limitation of claim 9 includes: wherein said upper surface for each said isolation trench **is formed** in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

Claim 7, in which claim 9 depends on, recites: planarizing with a single etch recipe the conformal layer to form therefrom an upper surface.... Therefore, the etch process of claim 9 is the **planarization process**.

According to the specification, page 14, lines 14-25, in the planarization of isolation film 36, film 36 (claimed conformal layer) is removed faster than the insulator island 22 (claimed first dielectric layer). Additionally, the claimed range 1:1 to about 2:1, further pointed to planarization.

The passage, page 15, lines 11-15, that the Applicants are referring to, is directed to the etch that removing the island 22, which does not include an etch rate and does not used to form the upper surface of the isolation trench.

The rejection is maintained.

With respect to the indefinite rejection of claims 21-23, since the "conductive" has been removed form the claims, the argument is moot.

Rejection under 35 U.S.C. 103(a)

With respect to '072, the Applicants assert: "In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse resist mask 368 over trench region 356 (?)..." then conclude: "Accordingly, the method disclosed in the '072 patent does not planarize the conformal oxide layer 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein".

Through out the arguments, Applicants fail to point out which limitation(s) that the references fail to teach. Note that, the limitations of the claims are "comprising", therefore, the many more process steps of the references have render the claims obvious.

Applicants' conclusion "the method disclosed in the '072 patent does not planarize the conformal oxide layer 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein" is erroneous. '072 patent clearly teaches a planarization (CMP) of the conformal oxide layer to form the structure as shown in Fig. 3M as "Finally the upper surface of the oxide layer 372, along with the oxide ridges 373, is polished by chemical/mechanical polishing (CMP)". (See col. 4, lines 47-62).

With respect to "planarization that is performed in the absence of masking of the conformal layer", even if the specification provides positive recitation to such issue, in which the instant specification does not, '072 patent clearly teaches that during the polishing, there is no mask present. **Applicants should point out where is the mask during the polishing of the oxide layer 372.**

Note that, the more complicated method does not means that '072 patent does not planarize the upper surface of the conformal oxide layer.

With respect to claim 34, '072 patent clearly teaches forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said oxide layer in contact with a pair of said spacers, and selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces. (See the rejections above).

With respect to claim 35, Applicant argues: "The '072 patent has no such teaching or suggest of this feature i.e., forming a polysilicon layer upon said oxide layer, of the invention".

As discussed above and many times previously, '072 clearly teaches "Also, a pad oxide containing a thin thermally-grown silicon oxide layer and a buffer polysilicon layer may be used for the pad oxide 340". (See col.4, ll. 14-16).

Applicant further adds: "claims 1, 7, 14, 18, 24-26, 31, 35, 38, and 42 recite some form of planarization that *is performed in the absence of masking of a conformal layer over at least one isolation trench*".

Note that, as discussed above, Applicants clearly try to claim what **he did not invent**.

After a careful review of the present specification, one can not find support for a "planarization that *is performed in the absence of masking of a conformal layer over at least one isolation trench*".

Applicant must and should point out the support for this new matter.

'072 patent in view of Poon or Wolf clearly render the claims obvious because thermal oxidizing the exposed trench to remove damage caused by the trench etch are well known in the art.

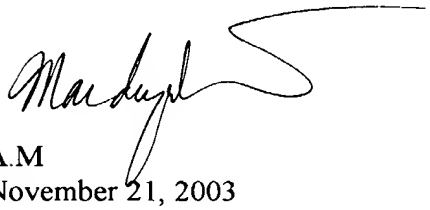
The claims are obvious over the combination of the references.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575 (or 571-272-1710 after January 13, 2003). The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



A.M
November 21, 2003